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# Performance of a 0.13 $\mu\text{m}$ SOI integrated 60 GHz dipole antenna

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## Abstract

This work presents the design of a 60 GHz fully integrated dipole antenna on 0.13  $\mu\text{m}$  silicon on insulator (SOI) substrate. A conductor backed coplanar waveguide balun has been designed on the top level layer to assure compatibility with the test devices. The CBCPW balun is completely characterized on SOI substrate for subsequent de-embedding of the antenna impedance. SOI substrate effect has been compensated by the introduction of an interdigitated capacitor to allow good dipole matching impedance at 60 GHz over a bandwidth of 8%. Backside substrate metallization has been used to improve radiation properties. The resulting simulated radiation efficiency is 85 % with a gain around 4.5 dBi.

## Introduction

With increasing use of coplanar waveguide (CPW) and related planar structures as transmission lines (TL) for MIC's and MMIC's, particularly at millimeters frequencies, there is a need for a complete family of compatible planar printed antennas. CPW fed antenna have received considerable attention recently [1, 2] due to the low radiation loss and less dispersion of the CPW TL with respect to microstrip TL. Over the last decades, technological advances have promoted exponential decrease in the size of computational functionality, rapid growth in the number of networked devices, diminishing wireless devices sizes and a continual decline in cost. The utilization of millimeter wave frequencies enables the design of compact, lightweight, and low cost wireless millimeter wave communication front-ends which can offer convenient terminal mobility and high capacity channel. A 60 GHz band is attractive candidate for short range radar and indoor communications based on Pico cell zone because it presents high atmospheric loss. Recently, Silicon on Insulator (SOI) technology was found to offer alternative solutions to many problems faced in the race to higher performance and low power of integrated devices [3]. The design of integrated antennas operating at 60 GHz is a critical issue when high efficiency is required. Such integrated antenna has low input impedance which doesn't match the conventional 50 Ohms devices. Special antenna design is required to compensate substrate effects. In addition, to feed a dipole by a coplanar RF-pad, a transition between coplanar Waveguide (CPW) and coplanar strip line (CPS) must be used for optimal design [1, 4].

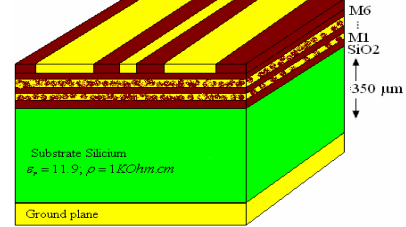
In this paper we describe the design of a CBCPW Transmission line (TL) integrated on SOI. After the characterization of the CPW TL, a balun is inserted to feed the interdigitated dipole antenna. The balun design and operation is discussed first, measurement and simulation results of the characterized balun are provided. Next the dipole design is considered, the measurement of the dipole and the de-embedding procedure is depicted. The discussion is concluded with the perspectives on codesign of the antenna with a low noise amplifier.

## I. Coplanar waveguide to coplanar strip “balun”

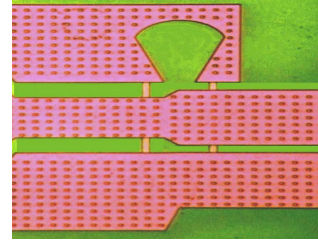
Coplanar waveguide (CPW) and coplanar strip line (CPS) are popularly used in the monolithic microwave integrated circuit (MMIC) devices since their uni-planar feature has some advantages such as easy fabrication, no need for via-holes, and easy integration with active

devices [5]. An effective interconnection between CPW and CPS TL must be cautiously designed to fully utilize their advantage, especially at very high frequency. A CPW to CPS transition circuit was designed to transform the unbalanced CPW feed line to a balanced CPS (balun) feed line in order to optimize the input of the balanced antenna [4].

CMOS bulk substrate includes a multi layer of metal, buried oxide structure and a low resistivity silicon substrate which generates high losses. However the recent introduction of high resistive substrate (SOI) reduces the dielectric losses, which prove the importance of SOI for the realization of low loss TL [6]. For the CPW TL, the unwanted even mode can be eliminated by the use of wire bonding or underpath connecting the two ground planes through vias. The topology of SOI substrate is as follows, a high resistive silicon layer (>1000 ohm.cm), six metals layers, buried oxide layer and finally a passivation layer (Fig. 1). The transition balun forms a good candidate for the antenna design since its operating bandwidth is much broader. The balun is composed of CPS & CPW TLs separated by a radial slot in the terminated ground, and 2 underpaths connecting the 2 ground planes (Fig. 2). Our objective is a 50 ohms input feed of the designed antenna. The characteristic impedance can be calculated basing on the conformal mapping method by using the formulas (1, 2) [7]



**Fig. 1 CPCPW on SOI**

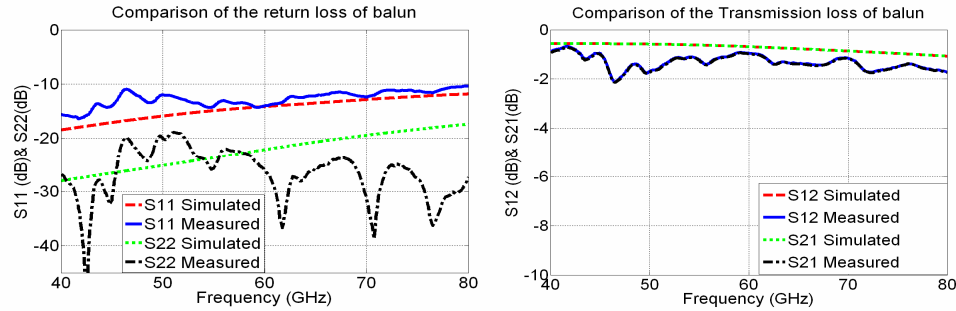


**Fig. 2 Balun on SOI**

$$Z_{0,CPW} = \frac{60\pi}{\sqrt{\epsilon_{eff}}} \frac{K(k)}{K(k')} \quad , \quad Z_{0,CPS} = \frac{120\pi}{\sqrt{\epsilon_{eff}}} \frac{K(k)}{K(k')} \quad (1,2)$$

Where

- $Z_{0,CPW}$ ,  $Z_{0,CPS}$ , are the characteristic impedance of the CPW & CPS TL
- $K$  is the elliptic integral of  $k$  and  $k'$  factor that depend on the dimensions of CPW & CPS (gap and central strip width)
- $\epsilon_{eff}$  is the effective permittivity of SOI



**Fig.3 Measured and simulated S parameters for the balun on SOI.**

The S parameters of the balun are measured using a HP8510XF vector network analyzer (Fig. 3). A TRL [8] calibrating kit was designed and measured to characterize the balun and to extract its characteristic impedance and its complex propagation constant. The reference impedance of this calibration is set to 50 ohms, and its reference plane is moved back to a position close to the probe tips using the port extension methods described in [9].

## II. Design of Dipole antenna

The dipole antenna is one of the most well-known and widely used radiating structures in RF applications. Different parameters can affect the properties of the dipole. The most important is the length which is inversely proportional to the frequency of operation. Another parameter is the

width which also influences the input impedance. An approximation of the length (L) of half wavelength dipole (fundamental resonating mode) is given by [10]:

$$L = 0.48 * \lambda ; \text{ Where } \lambda = \frac{c}{f \sqrt{\epsilon_{\text{reff}}}}$$

- $c$  is the speed of the light,
- $f$  is the frequency of operation,
- $\lambda$  is the wavelength and
- $\epsilon_{\text{reff}}$  is the effective permittivity of the substrate

The dipole is etched on the sixth layer (M6), which has a  $0.96 \mu\text{m}$  thickness. The input impedance of the antenna must be matched to the 50 Ohms by varying the length and width for a given substrate. The length and the width affect respectively the resonant frequency, and the resistance of the impedance ( $R_{\text{in}}$ ). The value of  $R_{\text{in}}$  is degraded due to high resistivity of the SOI substrate. For example, for a dipole of length =  $1250 \mu\text{m}$  and width =  $50 \mu\text{m}$ , the imaginary part of the input resistance shows two different resonant frequencies, a series resonance (47 GHz) and a parallel resonance (67 GHz) where  $R_{\text{in}}$  is equal to 15 Ohms and 215 Ohms respectively. Electromagnetic simulations confirm that increasing the width of the dipole decreases its input resistance. Figure 4 shows that by increasing the width from 40 to  $100 \mu\text{m}$ ,  $R_{\text{in}}$  falls from 215 to 137 Ohms. In the same time, the resonant frequency is shifted toward the low frequencies.

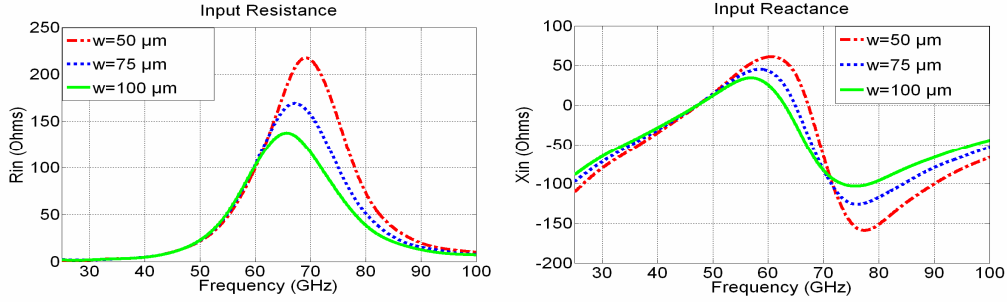


Fig. 4 Sweep of the width of the dipole antenna with  $L=1250 \mu\text{m}$

### III. Interdigitated Dipole Antenna

The input impedance of the half wavelength dipole at the fundamental resonance frequency can be modeled as inductance and a capacitance between the arms of the dipole. To compensate the substrate effect on the input impedance, a combination of techniques is directly implemented inside the dipole structure. In the first step, the arm width is increased to reduce the quality factor of resonance and obtain a wider operating bandwidth; in the second step, we take advantage of wide arms dipole to introduce an interdigitated structure [11] in order to mainly decrease the imaginary part of its input impedance. In addition to decrease the input reactance of the antenna, this interdigitated structure affects also its input resistance. The final 60 GHz fully integrated dipole antenna incorporating the interdigitated capacitor is realized on  $0.13 \mu\text{m}$  silicon on insulator (SOI) process, with following parameters : Dipole's length =  $742 \mu\text{m}$ , width =  $100 \mu\text{m}$ , width of the inter digit =  $6.25 \mu\text{m}$ . The arms of the dipole were hollowed out for technological reasons (Fig. 5).

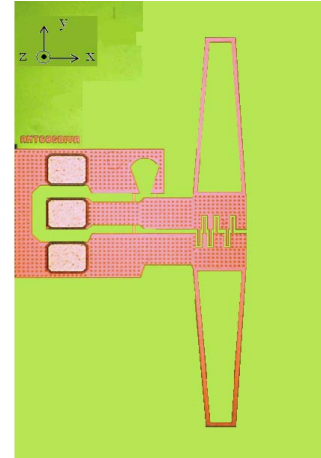
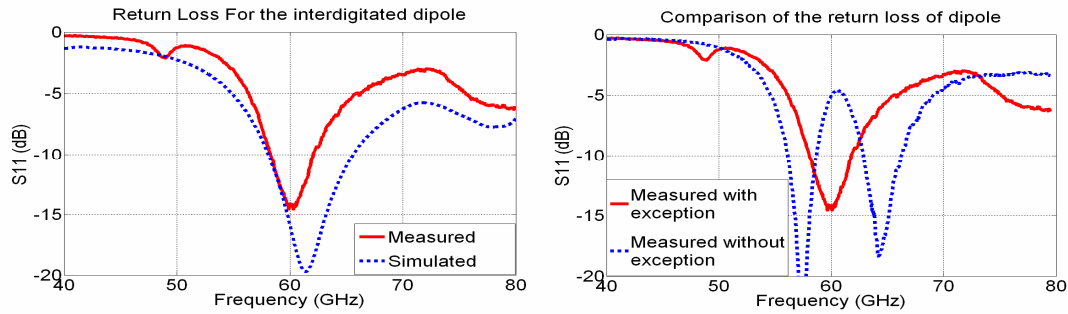


Fig. 5 Interdigitated antenna with balun

The design of the interdigitated dipole was based on electromagnetic simulations made using the CST Microwave Studio software package. The antenna was characterized experimentally using a HP 8510 XF vector network analyzer (VNA). Note that different technological exceptions have been applied particularly the metal exclusion zones for all layers, the holes in the M6 layers to respect metal density limitation, and the active silicon dummies layer that has been replaced by silicon dioxide. Fig (6.a) shows the comparison of the measured and the simulated return loss of the interdigitated hollowed dipole. It shows that the antenna exhibits a 15 dB return loss at 60 GHz with an 8% bandwidth at 10 dB. Figure (6.b) shows the comparison of the designed interdigitated dipole with (case a) and without exclusion

zones (case b). For the case b, the return loss shows that another resonance appears, corresponding to the propagation of complex resonant waves in the device.

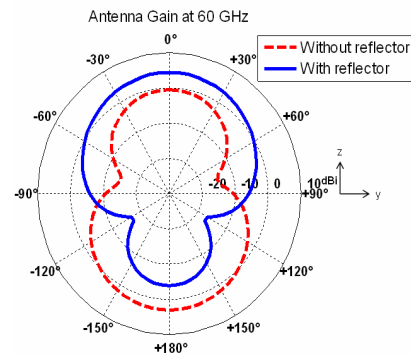


**Fig. 6 Case a) Return loss for the dipole**

**Case b) S11 with & without**

#### IV. Radiation pattern

The simulated radiation pattern of the interdigitated dipole is mainly directed toward the SOI substrate. With a backside metallization, the radiation pattern is the directed outward of the substrate. The distance between radiating arms and the reflector ( $355\mu\text{m} \sim \lambda_g/4$ ) is close to the optimal distance in order to add direct and reflected wave without any side lobes [10]. The simulated radiation efficiency is increased (85 % with a gain around 4.5 dBi (Fig. 7)). Measurements of antenna gain and radiation pattern are on the way...



**Fig.7 Gain pattern with and without reflector**

#### V. Conclusion

This paper has presented the design and preliminary measurement results for a 60 GHz interdigitated dipole antenna integrated on SOI. At 60 GHz the antenna exhibits a 15dB return loss. A difference of 5dB between the simulated and measured return loss is probably due to unconsidered technological parameters at 60GHz such as dummies, permittivity of SiO<sub>2</sub>, etc... The back side metallization under the wafer is used to act as a reflector. A radiation efficiency of 85% and a gain around 4.5 dBi are obtained. This antenna is a part of on chip design using CMOS SOI technology in order to be used in the co-design process of the antenna with a 60 GHz integrated Low Noise Amplifier.

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